REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

The Applicants appreciate the acknowledgement of allowable subject matter in claims 4 and 5.

By the foregoing amendment, claim 3 has been amended merely to correct a typographical error originally contained therein. Specifically, claim 3 has been amended to include a space on line 1 thereof, which was previously omitted. No new matter has been added. Thus, claims 1-14 are currently pending in the application and subject to examination.

Entry of this Amendment is proper under 37 C.F.R. § 1.116 since this Amendment: (a) places the application in condition for allowance for reasons discussed herein; (b) does not raise any new issue regarding further search and/or consideration since the Amendment amplifies issues previously discussed throughout prosecution; (c) does not present any additional claims without canceling a corresponding number of finally-rejected claims; and (d) places the application in better form for appeal, should an appeal be necessary. The Amendment is necessary because it is made in reply to 0arguments raised in the rejection. Entry of the Amendment is thus respectfully requested.

Objection to the Drawings

In the outstanding Office Action, Fig. 2 was objected to as failing to show reference numerals 17, 17' and 18, 18'. The specification has been amended in response to this objection. If any additional amendment is necessary to overcome the

objections and rejection, the Examiner is requested to contact the Applicant's undersigned representative.

Objection to the Claims

In the outstanding Office Action, claims 3, 8 and 9 were objected to as being in improper form. The Applicants respectfully traverse this objection, as follows.

Section 608.01(n) of the MPEP states that "any dependent claim which refers to more than one other claim ('multiple dependent claim') shall refer to such other claims in the alternative only. A multiple dependent claim shall not serve as a basis for any other multiple dependent claim." *MPEP § 608.01(n)*.

Claims 3, 8 and 9 refer to such other claims in the alternative only, and do not serve as a basis for any other multiple dependent claim. Thus, claims 3, 8 and 9 are in proper form.

Claim 3, however, has been amended to correct a typographical error as noted above. Specifically, claim 3 has been amended to include a space on line 1 thereof, which was previously omitted.

Rejections Under 35 U.S.C. § 103

Claims 1-3 and 8-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malcolm Jr. et al. (US Patent No. 6,373,954, hereinafter, "Malcolm") in view of Tsukamoto et al. (US Patent No. 4,815,352, hereinafter, "Tsukamoto"). Claims 6-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malcolm as modified by Tsukamoto, and further in view of Anderson (US Patent No. 6,078,594). It is noted that claim 3 has been amended. To the extent that the rejections remain

applicable to the claims currently pending, the Applicants hereby traverse the rejections, as follows.

Claims 1-13

In making these rejections, the Office Action asserts that Malcolm teaches "sequence control means (see fig. 1 121, 122, 120, such as first in, first out and see col. 11 line 57-62), bus interface means (101) for a common bus including an address bus and a data bus; bus master means (101) for issuing an address to said common bus through said bus interface means (101) under control of said sequence control means (116)..." Office Action, p. 3.

Thus, the Office Action first asserts that Malcolm teaches the claimed sequence control means by FIFO buffers 121, 122 and linear processing circuitry 120. Then, the Office Action asserts that Malcolm teaches the claimed sequence control means by FM synthesis circuit 116. However, FIFO buffers 121, 122 and linear processing circuitry 120 do not control the bus 101 (communication between the circuits 120, 121, 122 and the bus is one-way from the bus to those circuits). In addition, Malcolm neither discloses nor suggests that FM synthesis circuit 116 controls sequences in which the "bus master means" 101 issues addresses to a common bus.

Furthermore, the upper half of the codec 100 in figure 1 is an A/D conversion block and the lower half thereof is a D/A conversion block. Therefore, the portion of Malcolm that is of interest with respect to the present invention is the lower half, i.e., the D/A conversion block. Accordingly, in view of the direction of the arrow mark of Fig. 00 of Malcom, it is clear that the FIFO buffers 121, 122 and linear processing circuitry 120

do not control interaction between the FM synthesis circuit 116 and the bus interface/master means 101.

Thus, Malcolm does not disclose or suggest at least the sequence control means; bus interface means for a common bus including an address bus and a data bus; bus master means for issuing an address to said common bus through said bus interface means under control of said sequence control means, as recited in independent claim 1.

Tsukamoto discloses three channels in Figure 17 denoting "physical channels" because there are three D/As and three speakers in correspondence thereto. The three "physical channels" of Fig. 17 correspond to the monaural channel (one channel) in Figure 1 of the subject application and the stereo channels (right and left channels) in Figure 2. The sound channel of the claimed invention is not a physical channel, and indicates logical channels. Therefore, in the claimed invention, N*M logical channels are assigned to the single physical channel as clearly illustrated in Figs. 1 and 2 of the subject application.

In Tsukamoto, a single D/A is assigned to a single physical channel. In contrast, in the claimed invention, M sets of D/As are assigned to a single physical channel. In addition, in the claimed invention, N sets of time-divided-multiplexed sound channels (logical channels) are applied to each of the M sets of D/As. Therefore, in the claimed invention, N*M sound channels (logical channels) are allotted to the single physical channel.

Furthermore, in Tsukamoto, the demultiplexer assigns a plurality of slots being time-divided-multiplexed to any one of the three physical channels. In contrast, in the

claimed invention, all of the NxM sound channels (logical channels) are applied to the single physical channel.

The advantages performed by the present invention having the M sets of D/As are as follow: As shown in Figure 5 of the subject application depicting the claimed invention, there are provided four sets of D/As and a signal obtained by multiplexing data of four channels is input to each set of D/A. If only one set of D/A is provided and a signal obtained by multiplexing sixteen channels' data is input thereto, the sixteen channels' data are to be reproduced within the one period shown in Figure 5, and therefore, since the affective periods of the respective channels (period except for the no signal period) become shorter, efficiency of the D/A is significantly reduced. As a result, sound quality is also significantly reduced. However, if the four sets of D/As are provided as shown in Figure 5 depicting the claimed invention, the effective periods for the respective channels become longer, and therefore, the efficiency of the D/A is not reduced. All of the applied references are silent as to the above-described specific structure of the claimed invention; and therefore, advantages obtained by the specific structure of the claimed invention are similarly absent from the applied references.

As recited in claim 3, as amended, the digital/analog converting means is structured by a plurality of digital/analog converters and the digital/analog converters are provided in a cascade connection. Tsukamoto neither discloses nor suggests a cascade connection of the three D/As disclosed therein. Moreover, the three D/As disclosed by Tsukamoto respectively receive only the input signal from the demultiplexer. Thus, by the present invention as recited in claim 3, if the D/As are connected in a cascade fashion, it is possible to make the number of the bits of each

D/A smaller. As a result, it is possible to make the area of each D/A extremely small. For example, in a case that a 16-bit D/A is needed, in the present invention, two 8-bit D/A may be connected in a cascade fashion to be used as a 16-bit D/A. The area needed for the 8-bit D/A is approximately 1/256 of the area needed for a 16-bit D/A. Therefore, even if two 8-bit D/As are used, as recited in the claimed invention, the area necessary to implement the two 8-bit D/As is 2/256 of the area that would be necessary to implement a single 16-bit D/A. Thus, by connecting the D/As in a cascade fashion as recited in the claimed invention, the area needed for implementation of a semiconductor circuit, and, similarly, the cost for such a semiconductor circuit, may be decreased significantly.

Claim 14

Regarding claim 14, the Office Action asserts that Malcolm teaches the claimed first and second buses by ISA bus interface 101 and joystick logic 105. See Office Action, p. 7. However, joystick logic 105 does not comprise a second bus. Tsukamoto is not cited for, nor does Tsukamoto cure the deficiencies of Malcom noted above

To establish prima facie obviousness of a rejected claim, the applied art of record must teach or suggest each feature of a rejected claim. See M.P.E.P. §2143.03 and In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998). As explained above, none of the applied art of record, either alone or in combination, teaches or suggests each and every feature recited in independent claims 1 and 14.

Therefore, independent claims 1 and 14 are neither anticipated nor rendered obvious by the combination of Malcolm and Tsukamoto. Accordingly, the Applicants respectfully submit that independent claims 1 and 14 are patentably distinct over the

combination of Malcolm and Tsukamoto and in condition for allowance. As claim 1 is allowable, the Applicants submit that claims 2-13, which depend from allowable claim 1, are likewise allowable for at least the reasons set forth above with respect to claim 1.

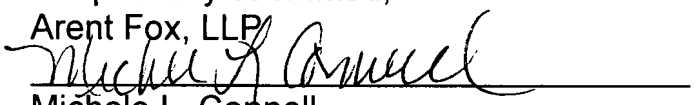
Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100341-00003.

Respectfully submitted,
Arent Fox, LLP



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